REMARKS

By the above amendment, the feature of dependent claim 2 has been incorporated into independent claim 1 and additionally the feature has been added that "the tips of the conductors terminate at a position of said one surface of said substrate so as to surround a periphery of said semiconductor chip with the bonding wires connecting the tips of the conductors with the bonding pads of said semiconductor chip", which feature is illustrated in Figs. 1 and 4 of the drawings of this application, wherein the tips of the conductors 4 terminate at a position on the substrate 8 surrounding a periphery of the semiconductor chip 2, with the bonding wires 13 connecting the tips of the conductors with the bonding pads 11 of the semiconductor chip, as illustrated in Fig. 4, for example. Additionally, such features have also been added to independent claims 7 and 12, and further, new dependent claims 17-19 have been presented which recite the feature that the conductors linearly extend in the radial pattern toward the semiconductor chip as clearly illustrated in Fig. 1, for example. Applicants submit that such features are not disclosed or taught in the cited art, as will become clear from the following discussion.

The rejection of claims 1-5, 7-10 and 12-15 under 35 U.S.C. 103(a) as being unpatentable over Ishikawa et al (US Patent 5,907,190) in view of Japanese patent 59105349 issued to Mori et al, and further in view of Eytcheson (US Patent 5,072,281) and the rejection of claims 6, 11 and 16 under 35 U.S.C. 103(a) as being unpatentable over the aforementioned combination of references in view of Irwin (US Patent 5,627,850), such rejections are traversed insofar as they are applicable to the present claims, and reconsideration and withdrawal of the rejections are respectfully requested.

As to the requirements to support a rejection under 35 U.S.C. 103, reference is made to the decision of In re Fine, 5 USPQ 2d 1596 (Fed. Cir. 1988), wherein the court

pointed out that the PTO has the burden under §103 to establish a prima facie case of obviousness and can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references. As noted by the court, whether a particular combination might be "obvious to try" is not a legitimate test of patentability and obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination. As further noted by the court, one cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention.

Furthermore, such requirements have been clarified in the recent decision of In re Lee, 61 USPQ 2d 1430 (Fed. Cir. 2002) wherein the court in reversing an obviousness rejection indicated that deficiencies of the cited references cannot be remedied with conclusions about what is "basic knowledge" or "common knowledge". The court pointed out:

> The Examiner's conclusory statements that "the demonstration mode is just a programmable feature which can be used in many different device[s] for providing automatic introduction by adding the proper programming software" and that "another motivation would be that the automatic demonstration mode is user friendly and it functions as a tutorial" do not adequately address the issue of motivation to combine. This factual question of motivation is immaterial to patentability, and could not be resolved on subjected belief and unknown authority. It is improper, in determining whether a person of ordinary skill would have been led to this combination of references, simply to "[use] that which the inventor taught against its teacher."... Thus, the Board must not only assure that the requisite findings are made, based on evidence of record, but must also explain the reasoning by which the findings are deemed to support the agency's conclusion. (emphasis added)

Applicants note, that as indicated above, claim 1 as well as the other independent claims 7 and 12 have been amended to incorporate the feature of

dependent claim 2 therein, that a largest pitch of the tips of the conductors of two adjacent conductors at the vicinity of each of the four corners of the semiconductor chip is less than twice a smallest pitch with respect to pitches of respective tips of the plurality of conductors surrounding the semiconductor chip. With this structural arrangement, supporting leads to which bonding wires are not connected at the four corner portions of the semiconductor chip are eliminated, and the area previously occupied by supporting leads becomes a further area for arranging the conductors at the vicinity of the corner portions of the semiconductor chip and a large number of pins of a package device can be utilized, noting the diagonal extension of such conductors. Further, as now recited in the claims, the tips of the conductors terminate at a position on the substrate so as to surround a periphery of the semiconductor chip with the bonding wires connecting the tips of the conductors with the bonding pads of the semiconductor chip and the mechanical stability of the tips of the conductors is increased so that the width of the conductors can be reduced and the length of the bonding wires connecting the tips of the conductors and bonding pads of the semiconductor chip can be reduced, whereby high speed packaging of the device is improved. Moreover, as recited in independent claims 7 and 12, the bonding pads have an arrangement so that a pitch of the bonding pads at the corners of the chip is wider than a pitch of the bonding pads at other portions of the chip. With this construction, undesirable wire flow at the four corners of the resultant resin body can be decreased at the time of the resin molding step and electrical reliance of the package device can be achieved. Thus, a package device with a large number of pins which is achieved with high speed and high electrical reliance can be provided. Applicants submit that such features as recited in the independent and dependent claims of this application are not disclosed or taught in the cited art.

With regard to Ishikawa et al, the Examiner recognizes that this patent does not disclose a pitch between adjacent bonding pads increases in a direction toward

four corners defined by the four sides of the main surface of the chip and does not expressly disclose the chip as a quadrilateral shape and wires along the four sides. Assuming arguendo that Ishikawa et al provides a chip with a quadrilateral shape and wires along the four sides, applicants submit that there can be no question that Ishikawa et al also does not disclose or teach that the plurality of conductors are arranged so as to extend with one respective end thereof in a radial pattern toward the semiconductor chip such that an extension of the one respective end of at least one of the plurality of conductors extends diagonally through a corner of the semiconductor chip. The Examiner recognizing some of the deficiencies of Ishikawa et al cites the Japanese patent to Mori et al, indicating that Fig. 3 of this reference shows that the pitch between adjacent bonding pads d1-d13 of the quadrilateral shape chip "a" increases in a direction toward four corners defined by the four sides of the main surface of the chip. Irrespective of this disclosure, it is readily apparent from Fig. 1 of the drawings of the Japanese patent to Mori et al, that the plurality of conductors b are not arranged so as to extend with one respective end thereof in a radial pattern toward the semiconductor chip with the Examiner at least acknowledging that "The Japanese patent, or the Ishikawa reference, does not disclose an extension of the one respective end of at least one of the plurality of conductors extends diagonally through a corner of the chip". Thus, applicants submit that in addition to the recognized deficiencies of the Japanese patent and Ishikawa et al, neither reference discloses the radial pattern as defined and other features, as will be discussed, such that each of the independent claims patentably distinguish over this proposed combination of references in the sense of 35 U.S.C. 103 and should be considered allowable thereover.

The Examiner recognizing the deficiencies of the Japanese patent and Ishikawa et al at least with respect to the extension of the one respective end of at least one the plurality of conductors extends diagonally through a corner of the chip cites Eytcheson as disclosing such feature. The Examiner indicates that Eytcheson

discloses in figure 2, extension of conductive leads 14 extends diagonally through a corner of chip 10, as shown in the figure. Therefore, the Examiner concludes it would have been obvious to one of ordinary skill in the art at the time the invention was made to make one of the conductors of the Ichikawa in view of the Japanese patent device to extend diagonally through a corner of the chip therein in order to have greater flexibility in accessing the individual circuitry components on the chip. Applicants submit that the Examiner has engaged in a hindsight reconstruction attempt utilizing the principle of "obvious to try" which is not the standard of 35 U.S.C. 103. See In re Fine, supra.

In formulating the combination of Eytcheson with the Japanese patent and Ishikawa et al, the Examiner destroys the teaching of Ishikawa et al and the Japanese patent to utilize bonding wires, as recited in each of the independent claims of this application, to connect the tips of the conductors with the bonding pads of the semiconductor chip. That is, in Eytcheson, the electrically conductive leads 14, if assumed to be electrical conductors, as recited in the claims of this application, eliminate the utilization of bonding wires and are directly connected to the bonding pads 18 of the semiconductor chip or integrated circuit device 10. Moreover, if the Examiner contends that the electrical leads 14 represent bonding wires, then it is apparent that the plurality of conductors to which the electrical leads 14 are connected at the opposite end thereof with respect to the bonding pads 18 are not arranged in a radial pattern in the manner recited in each of the independent claims of this application and do not have an extension of one respective end thereof which extends diagonally through a corner of the chip. As such, applicants submit that each of the independent claims of this application as previously presented patentably distinguish over this proposed combination of references in the sense of 35 U.S.C. 103 and should be considered allowable thereover.

As noted above, by the present amendment, the features of dependent claim 2 have been incorporated into independent claim 1, with the similar features being

incorporated into independent claims 7 and 12. Applicants note that dependent claim 2 recites the feature that "a largest pitch of the tips of the conductors of two adjacent conductors at the vicinity of each of the four corners of said semiconductor chip is less than twice a smallest pitch with respect to pitches of respective tips of said plurality of conductors surrounding said semiconductor chip" (emphasis added). That is, this feature relates to the pitch of the tips of the conductors 4 in relation to the corners of the semiconductor chip and not a relation of the pitch of the bonding pads of the semiconductor chip. The Examiner refers to the last paragraph of the abstract of the Japanese patent which indicates that based on an optimum value, which is determined by successive approximation with a computer, the increasing intervals are determined. Applicants note that such description in the Japanese patent to Mori et al relates to the bonding pads of the semiconductor chip, noting that the abstract of the Japanese patent provides "For example, the arrangement of 13 bonding pads...is made on one side of a chip, and, based on the optimum value, the pad intervals are successively enlarged toward each corner from the center of one side of the chip thereby enabling the arrangement in such a manner that each wire interval becomes almost constant". (emphasis added) Thus, it is apparent that the description relates to the pitch of bonding pads and not to the pitch of conductors as recited in claim 2 and as recited now in each of independent claims 1, 7 and 12 of this application.

As to the Examiner's contention that "it would have been obvious to one of ordinary skill in the art at the time the invention was made to determine the pitch (increasing intervals) in order to have more exact constant wire intervals", applicants submit that such position of the Examiner has no relation to pitch of conductors and further the Japanese patent provides no disclosure of teaching of the specific relationship as set forth in terms of the pitch. Thus, applicants submit that the proposed combination fails to provide the claimed features and any suggestion that it would be obvious to provide such feature, represents a utilization of the teachings of

applicant against applicant which is not proper. See In re Lee, supra. In this regard, it is noted that Eytcheson also provides no disclosure or teaching of such recited features. Accordingly, applicants submit that the proposed combination of references fails to provide the aforementioned recited features which are recited in each of independent claims 1, 7 and 12 and the dependent claims thereof, such that all claims patentably distinguish thereover and should be considered allowable at this time.

Applicants note that each of the independent claims has also been amended to recite the feature that the tips of the conductors terminate at a position on the one surface of the substrate so as to surround a periphery of the semiconductor chip with the bonding wires connecting the tips of the conductors with the bonding pads of the semiconductor chip. Although the Examiner has cited Eytcheson for apparently disclosing an extension of a conductor which extends diagonally through a corner of a chip, as pointed out above, the electrical leads 14, if considered to be conductors which may have the aforementioned feature, eliminate the utilization of bonding wires and therefore cannot be properly combined with Ishikawa et al and the Japanese patent. Furthermore, it is readily apparent since these leads 14 terminate at the bonding pads 18 of the semiconductor chip, Eytcheson fails to provide the aforementioned claimed feature, which is now present in each of independent claims 1, 7 and 12, such that the recited features of the independent claims further patentably distinguish over the proposed combination of references as suggested by the Examiner in the sense of 35 U.S.C. 103, and all claims should be considered allowable thereover.

With respect to dependent claims 5, 9, 10, 14 and 15, the Examiner recognizes that such recited features are not disclosed in the cited art, contending that it would be obvious to provide such features. Further, the Examiner has recognized that the features of dependent claim 3 and other dependent claims are not disclosed or taught. Hereagain, the Examiner has engaged in a hindsight

reconstruction attempt utilizing applicants' disclosure which is not proper. See In re Fine, supra and In re Lee, supra. Thus, applicants submit that these dependent claims, when considered in conjunction with the parent claims, further patentably distinguish over the cited art in the sense of 35 U.S.C. 103, and should be considered allowable thereover.

As to the rejection of claims 6, 11 and 16 based upon the aforementioned combination of references further in view of Irwin et al, irrespective of the Examiner's position concerning Irwin et al, this patent does not overcome the aforementioned described deficiencies of the proposed combination of references and applicants submit that claims 6, 11 and 16 also patentably distinguish over this proposed combination of references irrespective of the teaching of Irwin et al. Thus, these dependent claims should also be considered allowable at this time.

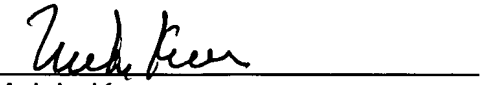
With respect to newly added claims 17-19, such claims recite the feature that the conductors linearly extend in the radial direction and applicants note that Eytcheson specifically provides that the electrical conductors 14 are formed so as to have an arcuate shape 16 at the region where the lead 14 is bonded to the integrated circuit 10, with the arcuate shape 16 being generally of similar length and disposed so as to all rotate generally in the same direction around the integrated circuit 10. Thus, it is readily apparent that Eytcheson specifically discloses a structure contrary to that claimed in dependent claims 17-19, and such claims further patentably distinguish over the cited art and together with the parent claims should be considered allowable at this time.

In view of the above amendments and remarks, applicants submit that all claims present in this application should now be in condition for allowance, and issuance of an action of a favorable nature is courteously solicited.

To the extent necessary, applicant's petition for an extension of time under 37 CFR 1.136. Please charge any shortage in the fees due in connection with the filing

of this paper, including extension of time fees, to Deposit Account No. 01-2135 (501.35250CX3) and please credit any excess fees to such deposit account.

Respectfully submitted,



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